Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 75-115 as follows:

Listing of Claims:

Claims 1-74 (Cancelled)

75. (New) An active termination circuit for setting the input impedance of a plurality of terminals to a predetermined value, the active termination circuit comprising:

a respective first controllable impedance device coupled between a first supply voltage and each of the terminals, the impedance of the first controllable impedance device being controlled by an impedance control signal;

a control circuit coupled to provide the impedance control signal to all of the first controllable impedance devices, the first control circuit comprising:

a second controllable impedance device coupled between a second supply voltage and a feedback node, the second controllable impedance device being a different controllable impedance device from the first controllable impedance devices, and the feedback node being different from one of the terminals, the impedance of the second controllable impedance device being controlled by the impedance control signal;

a predetermined resistance coupled between the feedback node and a third supply voltage, the second controllable impedance device and the predetermined resistance forming a voltage divider between the second and third supply voltages to produce a feedback voltage at the feedback node; and

a circuit generating the impedance control signal as a function of the feedback voltage so that magnitude of the feedback voltage is substantially constant.

76. (New) The active termination circuit of claim 75 wherein the circuit generating the impedance control signal comprises a comparator circuit comparing the feedback

voltage to a reference voltage, the comparator circuit causing the impedance control signal to vary so that the feedback voltage is substantially equal to the reference voltage.

77. (New) The active termination circuit of claim 76 wherein the comparator circuit comprises a first differential amplifier generating a comparison signal corresponding to the difference between the feedback voltage and the reference voltage, the impedance control signal corresponding to the comparison signal.

78. (New) The active termination circuit of claim 75 wherein the control circuit is operable to provide a common impedance control signal to all of the first controllable impedance devices.

79. (New) The active termination circuit of claim 75 wherein the first and second supply voltages have the same magnitude.

80. (New) The active termination circuit of claim 79 wherein the first and second supply voltages comprise a power supply voltage.

81. (New) The active termination circuit of claim 80 wherein the third supply voltage comprises ground potential.

82. (New) The active termination circuit of claim 75 wherein the control circuit is operable to generate the impedance control signal to maintain the impedance of the second controllable impedance device substantially equal to the impedance of the predetermined resistance.

83. (New) The active termination circuit of claim 75 wherein the first controllable impedance device and the second controllable impedance device comprise identical controllable impedance devices.

84. (New) The active termination circuit of claim 83 wherein the first controllable impedance device and the second controllable impedance device comprise identical MOSFET transistors.

85. (New) The active termination circuit of claim 75 wherein the first and second controllable impedance devices comprises respective voltage controlled impedance devices.

86. (New) The active termination circuit of claim 75 wherein the active termination circuit is fabricated in an integrated circuit device, and wherein the terminals having their impedance set by the active termination circuit comprise terminals that are externally accessible from outside the integrated circuit.

87. (New) A memory device, comprising:

a command decoder receiving memory command signals through externally accessible command input terminals, the command decoder generating memory control signals responsive to predetermined combinations of the command signals;

an address decoder receiving address signals through externally accessible address input terminals, the address decoder generating row and column addressing signals responsive to the address signals;

at least one memory array, the at least one memory array writing data to and reading data from locations corresponding the address signals responsive to the memory control signals;

a data path extending between a plurality of externally accessible data bus terminals and the memory array for coupling data signals to and from the memory array; and

an active termination circuit for setting the input impedance of plurality of the externally accessible terminals to a predetermined value, the active termination circuit comprising:

a respective first controllable impedance device coupled between a first supply voltage and each of the externally accessible terminals, the impedance of the first controllable impedance device being controlled by an impedance control signal;

a second controllable impedance device coupled between a second supply voltage and a feedback node, the second controllable impedance device being a different controllable impedance device from the first controllable impedance devices, and the feedback node being different from one of the externally accessible terminals, the impedance of the second controllable impedance device being controlled by the impedance control signal;

a predetermined resistance coupled between the feedback node and a third supply voltage, the second controllable impedance device and the predetermined resistance forming a voltage divider between the second and third supply voltages to produce a feedback voltage at the feedback node; and

a circuit generating the impedance control signal as a function of the feedback voltage so that magnitude of the feedback voltage is substantially constant.

88. (New) The memory device of claim 87 wherein the circuit generating the impedance control signal comprises a comparator circuit comparing the feedback voltage to a reference voltage, the comparator circuit causing the impedance control signal to vary so that the feedback voltage is substantially equal to the reference voltage.

89. (New) The memory device of claim 88 wherein the comparator circuit comprises a first differential amplifier generating a comparison signal corresponding to the difference between the feedback voltage and the reference voltage, the impedance control signal corresponding to the comparison signal.

90. (New) The memory device of claim 87 wherein the control circuit is operable to provide a common impedance control signal to all of the first controllable impedance devices.

91. (New) The memory device of claim 87 wherein the first and second supply voltages have the same magnitude.

92. (New) The memory device of claim 91 wherein the first and second supply voltages comprise a power supply voltage.

93. (New) The memory device of claim 92 wherein the third supply voltage comprises ground potential.

94. (New) The memory device of claim 87 wherein the control circuit is operable to generate the impedance control signal to maintain the impedance of the second controllable impedance device substantially equal to the impedance of the predetermined resistance.

95. (New) The memory device of claim 87 wherein the first controllable impedance device and the second controllable impedance device comprise identical controllable impedance devices.

96. (New) The memory device of claim 95 wherein the first controllable impedance device and the second controllable impedance device comprise identical MOSFET transistors.

97. (New) The memory device of claim 87 wherein the first and second controllable impedance devices comprises respective voltage controlled impedance devices.

98. (New) The memory device of claim 87 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.

99. (New) The memory device of claim 87 wherein the memory device comprises a dynamic random access memory.

100. (New) The memory device of claim 99 wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

101. (New) A computer system, comprising:

an integrated circuit processor having a plurality of externally accessible terminals coupled to a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

an integrated circuit memory device a plurality of externally accessible terminals coupled to a processor bus; and

an active termination circuit coupled to at least some of the externally accessible terminals, the active termination circuit comprising:

a respective first controllable impedance device coupled between a first supply voltage and each of the externally accessible terminals, the impedance of the first controllable impedance device being controlled by an impedance control signal;

a second controllable impedance device coupled between a second supply voltage and a feedback node, the second controllable impedance device being a different controllable impedance device from the first controllable impedance devices, and the feedback node being different from one of the externally accessible terminals, the impedance of the second controllable impedance device being controlled by the impedance control signal;

a predetermined resistance coupled between the feedback node and a third supply voltage, the second controllable impedance device and the predetermined resistance forming a voltage divider between the second and third supply voltages to produce a feedback voltage at the feedback node; and

a circuit generating the impedance control signal as a function of the feedback voltage so that magnitude of the feedback voltage is substantially constant.

102. (New) The computer system of claim 101 wherein the circuit generating the impedance control signal comprises a comparator circuit comparing the feedback voltage to a reference voltage, the comparator circuit causing the impedance control signal to vary so that the feedback voltage is substantially equal to the reference voltage.

103. (New) The computer system of claim 102 wherein the comparator circuit comprises a first differential amplifier generating a comparison signal corresponding to the difference between the feedback voltage and the reference voltage, the impedance control signal corresponding to the comparison signal.

104. (New) The computer system of claim 101 wherein the control circuit is operable to provide a common impedance control signal to all of the first controllable impedance devices.

105. (New) The computer system of claim 101 wherein the first and second supply voltages have the same magnitude.

106. (New) The computer system of claim 105 wherein the first and second supply voltages comprise a power supply voltage.

107. (New) The computer system of claim 106 wherein the third supply voltage comprises ground potential.

108. (New) The computer system of claim 101 wherein the control circuit is operable to generate the impedance control signal to maintain the impedance of the second

controllable impedance device substantially equal to the impedance of the predetermined resistance.

109. (New) The computer system of claim 101 wherein the first controllable impedance device and the second controllable impedance device comprise identical controllable impedance devices.

110. (New) The computer system of claim 109 wherein the first controllable impedance device and the second controllable impedance device comprise identical MOSFET transistors.

111. (New) The computer system of claim 101 wherein the first and second controllable impedance devices comprises respective voltage controlled impedance devices.

112. (New) The computer system of claim 101 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.

113. (New) The computer system of claim 101 wherein the memory device comprises a dynamic random access memory.

114. (New) The computer system of claim 113 wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

115. (New) The computer system of claim 101 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.